1.0 **REMARKS/ARGUMENTS**

1.1 **Introductory Remarks**

Previously filed claims Claims 1-13 have been amended as follow by this Amendment: Claims 1-8, 10, and 12-13 remain as a result of this Amendment. In particular, Claims 1, 6, 10, 12, and 13 have been amended, while Claims 9 and 11 have been cancelled without prejudice. Claims 2-5 and 7-8 are original claims also pending.

1.2 **Summary of Claim Amendments and Support**

By this Amendment, Applicant respectfully requests Examiner to cancel Claims 9 and 11 without prejudice. Please also amend Claims 1, 6, 10, 12, and 13, while Claims 2-5 and 7-8 remain unchanged and are original claims. Applicant respectfully submits that the amended claims provided do not introduce new matter. Support for amended Claims is provided in the originally filed Application, and specific references are cited below as examples of support, and accordingly no new matter is being introduced. Moreover, the sample of cited of references is not meant to reflect a complete listing of all instances of support from the originally filed Application.

Currently amended and pending Claims are provided as follows as a matter of convenience, annotated in bold for emphasis with reference support from the originally filed application.

1. (Currently Amended) An integrated multi-chip connector module comprising:

an array of substrate assemblies, wherein each substrate assembly comprises:

a substrate;

one or more ~~integrated circuits~~ semiconductor dice **(318, p. 5, lines 3-9)** attached to the substrate;

a set of input connector pins, each input connector pin further comprising a first end and a second end, wherein the first end is provided to receive an incoming signal, and the second end is electrically connected to the one or more ~~integrated circuits~~ semiconductor dice **(318, p. 5, lines 5-9)** on the substrate; and

a set of output connector pins, each output connector pin further comprising a first and a second end, wherein the first end is electrically connected to the one or

more ~~integrated circuits~~ s miconductor devices (318, p. 5, lines 5-9), and the second end is provided f r transmitting a processed signal from the one or more ~~integrated circuits~~ semis nductor devices (318, p. 5, lines 5-9) as an output signal to the second end of each output connector pin; and

a connector housing or encasing the array of substrate assemblies, wherein the housing com rises a first set of signal pin apertures through which extend the set of i put connector pins to allow external electrical connection to a first exte nal device, and wherein the housing further comprises a second set o signal pin apertures through which extend the set of output connector pins o allow external electrical connection to a second external device, wherein he connector housing further comprises injection-molding a thermally con uctive composite around the array of substrate assemblies to fill a plura ity of cavities between the array of substrate assemblies, the injection molded connector housing (p. 10, line 31 to p. 11, lines 1-2) thereby fo ming a semiconductor packaging (p. 5, lines 18-20) for the one or more s miconductor dice while securing in place the array of substrate assem lies, the one or more semiconductor dice, and the plurality of input and o put connector pins (p. 10, line 31 to p. 11, lines 1-2).

Claims 2-5 are originally filed claims, and not amended by this Amendment.

6. (Currently Amended) The integrated multi-chip connector module of Claim 1 wherein the one or more ~~integrated cir~~ uits semiconductor devices (p. 6, lines 8-9, 13-21) receive a first set of data signals at a f st electrical voltage level and generate in response a set of output signals comprising the irst set of data signals at a second electrical voltage level.

Claims 7-8 are originally filed claims, and thus remain unchanged by this Amendment.

Claim 9 is cancelled without p rejudice.

10. (Currently Amended) An i tegrated multi-chip connector module assembly method comprising:

assembling one or more ~~integra ed circuits~~ semiconductor dice (p.7, lines 6-12) on a substrate frame;

attaching a plurality of connect r pins to each substrate frame and electrically connecting each connector pin to the one o more ~~integrated circuits~~ semiconductor dice (p.7, lines 6-12) on each substrate frame t transmit processed signals from the one or more ~~integrated circuits~~ semiconduct r dice;

stacking into an array a plurali y of the substrate frames to form an ~~assembly~~ array of substrate frames; and

encasing the stacked array of s bstrate frames in a connector housing, wherein the step of encasing the stacked array com rises injection molding a thermally conductive composite around the stacked array (p. 10 line 31 to p. 11, lines 1-2) to eliminate a plurality of cavities between the array of s bstrates to form a semiconductor packaging around the one or more semiconductor die (p. 5, lines 18-20) and securing in place the stacked array, the one or more semicon luctor dice, and the plurality of input and output connector pins(p. 10, line 31 t p. 11, lines 1-2).

Claim 11, an originally filed de pendent Claim has been cancelled without prejudice, its limitation having been combined with Claims 1 and 10.

Claims 12-13 have minor amen dments to renumber Claim number dependency as a result of cancellation of Clair s.

As provided above, specific re erences to supporting cites from the originally filed application have been pro vided for amended Claims recited above, and thus Applicant respectfully submits that no new matter has been introduced in this Amendment.

1.3 Specification: An ndment To Title Of Invention

Examiner has required a more descriptive title, and Applicant respectfully acknowledges this request and submits that an amendment to the Title of this Application has been made, with the amend d Title:

"A Multi-Chip Connector Mc dule Having One Or More Semiconductor Dice"

1.4 Rejections Under 02(b): Anticipation By Paagman (US Pat 5924899)

Examiner has rejected laims 1-2 and 5-13 as being anticipated by Paagman. To establish anticipation, a cite l reference must teach each and every aspect of the claimed invention, either expli tly or implicitly. Moreover, a claim is anticipated only if each and every element as set f rth in a claim is found, either explicitly or inherently, in a single prior art reference. Furt ermore, the identical invention must be shown in as complete detail as is contained n the claim. Hence, where even one aspect of the claim is not found in a prior art refer ice, such reference does not anticipate the claimed invention. In addition, to antic pate, the reference must also enable one of skill in the art to make and use the claimed in vention, thus placing the allegedly disclosed matter in the possession of the public, claim d by Applicant.

Applicant respectfully ubmits that the currently amended set of claims obviates the Examiner's rejec on. Moreover, even if currently amended claims were viewed in light of Paagm n, no where in the Paagman reference is shown or taught Applicant's claimed fea ure as in Claim 1:

> wherein the connector housing further comprises injection-molding thermally conductive composite around the array of substrate assemblies to fill a plurality of cavities between the array of substrate assemblies, the injection-molded connector housing thereby forming a semiconductor packaging for the one or more semiconductor dice while securing in place the array of substrate assemblies, the one or more semiconductor dice, and the plurality of input and output connector pins.

Recited in part from amended Claim 1.

In particular, support or amended Claim 1 is provided on page 5 lines 18-20, wherein Applicant dis ctly points out as a particular feature of this invention, the "Electrical conn ector 120 thus also serve as packaging integrated semiconductor die 318." Mor over, as an example in describing one

embodiment and assembly of connector 120 on page 10, line 31, to page11, lines 1-2,

> ...Substrate assembly 400 also comprises cavities 424, 428 that will be filled with injected plastic during electrical connector assembly to lock an array of substrate assembly 400 in place to form the internal structure and array of semiconductor dice and connector pins in place.

Conversely, Paagman's connector comprises housing 46 having slots created between dividing walls 53 to allow an interference fit of circuit substrate module 24 (Paagman, col 3, lines 27-35.) Moreover, Paagman teaches providing spaces 62 between each module to allow space for mounted components. (Paagman, col. 3, lines 35-37.) In contrast, as provided in Applicant's application and claims, an objective of Applicant's electrical connector 120 is to provide a semiconductor packaging for the one or more semiconductor dice, such as through injection molding plastic around the substrate assemblies, thereby filling in cavities between the substrate array, sealing and protecting the one or more semiconductor dice, while also securing in place the substrate arrays and pins to form the internal structure of the connector. Nowhere in Paagman is shown or taught this feature as part of Paagman's connector housing. Accordingly, Applicant respectfully submits that amended Claim 1 is allowable for the reason provided.

Claims 2-8 are dependent from amended Claim1, and for the reasons provided above with regards to the allowance of Claim 1. Applicant also submits that Claims 2-8 are now in condition for allowance.

Claim 9 has been cancelled.

Claim 10, as currently amended, recited for convenience as follows:

10. (Currently Amended) An integrated multi-chip connector module assembly method comprising:

assembling one or more ~~integrated circuits~~ semiconductor dice on a substrate frame;

attaching a plurality of connector pins to each substrate frame and electrically connecting each connector pin to the one or more ~~integrated circuits~~ semiconductor dice on each substrate frame to transmit processed signals from the one or more ~~integrated circuits~~ semiconductor dice;

stacking into an array a plurality of the substrate frames to form an ~~assembly~~ array of substrate frames; and

encasing the stacked array of substrate frames in a connector housing, wherein the step of encasing the stacked array comprises injection molding a thermally conductive composite around the stacked array to eliminate a plurality of cavities between the array of substrates to form a semiconductor packaging around the one or more semiconductor dice and securing in place the stacked array, the one or more semiconductor dice, and the plurality of input and output connector pins.

As similarly discussed above with regards to amended Claim 1, no where in the Paagman reference is shown or taught the step of injection molding around the array of substrate assemblies to seal the one or more semiconductor dice and to lock the array of assemblies and input/output pins to thereby form both a semiconductor packaging for the one or more semiconductor dice, as well as securing the internal structure of pins and arrays of assemblies.

Claim 11, an originally filed Claim describing injection molding step to form the connector housing has been cancelled since this feature is now combined with Claims 1 and 10.

As to Claims 12 and 13, dependent from amended Claim 10, Applicant respectfully submits that the reasons provided above supporting allowance of amended Claim 10 also therefore supports allowance for dependent Claims 12-13.

1.5 Claim Rejection Under 103(a) over Paagman

Examiner also rejected Claims 3-4 as being obvious under 103(a) over Paagman.

Applicant respectfully submits that Claim 3-4 are dependent claims from Claim 1, and as such, the foregoing arguments supporting allowance of amended Claim 1 also supports allowance of dependent Claims 3 and 4.

1.6 **CONCLUSION**

Claims 1-8, 10, and 12-13 are pending in this application. It is respectfully submitted by Applicant that no new matter has been introduced by this Amendment. Applicant further submits that the pending claims, Claims 1-8, 10 and Claims 12-13 are allowable for the reasons discussed above and requests a quick allowance of these claims. Should the Examiner have any remaining issues that may be expeditiously resolved, Applicant respectfully requests the Examiner to contact the undersigned at 650.280.0523.

Respectfully submitted,
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